UNIVERSITY OF JOHANNESBURG

**NAME AND SURNAME** :_____

**STUDENT NUMBER** :_____

**PROGRAM** : BACHELOR OF ENGINEERING TECHNOLOGY [**BEng Tech**] IN ELECTRICAL ENGINEERING. B6ELEQ & B6ELXQ

**MODULE** : **Digital Technology B2 – MAIN**

**CODE** : **DIGELB2**

**DATE** : SUMMER MAIN EXAMINATION NOVEMBER 2019

**DURATION** : 3 HOURS

**CALCULATION CRITERIA** : 40 [SEMESTER]: 60 [EXAM]

**NQF** : 7

**TOTAL MARKS** :100

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**EXAMINER** : Mr. J Venter

**MODERATOR** : Mrs. J Buisson-Street

**NUMBER OF PAGES** : 9 PAGES

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**INSTRUCTIONS** : FILL IN ANSWERS ON THE QUESTION PAPER.

**REQUIREMENTS** : NONE

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2/…

**INSTRUCTIONS TO CANDIDATES:**

1. 100 MARKS = 100%.
2. ATTEMPT ALL QUESTIONS.
3. ANSWER QUESTIONS CONSIDERING THE MARK ALLOCATION.
4. QUESTIONS MAY NOT BE ANSWERED IN ANY ORDER AND **ALL PARTS OF A QUESTION MUST BE KEPT TOGETHER**.
5. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND LABELED CLEARLY.
6. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
7. **MARKS WILL BE DEDUCTED** FOR WORK WHICH IS POORLY PRESENTED.
8. ANSWER ALL THE QUESTIONS.

**QUESTION 1 PIC QUESTIONS**

1.1 Justify three (3) ways that PIC/Arduino implementations can be powered with regards to power consumption and mobility. (6)

1.2 In your own words explain why are flow charts used in the designing of PIC projects. (2)

1.3 Explain why is a pull-up or pull-down resistor necessary in a PIC/Arduino circuit. (2)

1.4 For a digital input, where the maximum and minimum values are 9 V and 0 V, decide what the output will be when the input is the following (answer only LOW or HIGH or UNDEFINED) (4)

1.4.1 1 V

1.4.2 4.5 V

1.4.3 6 V

1.4.4 7.5 V

1.5 Predict the outcome of the *if* tests, below, will be when the value of x is 0 (answer only TRUE or FALSE). (2)

1.5.1 If (x=0) then …

1.5.2 If (x==0) then …

1.6 Compile a code that will allow the reception of an analogue input and print this information to a device using the serial port for **a 0 – 5 V input**. You may use C-coding or Arduino coding only.

The baud rate must be **19200 bps**. The pin where the analogue value is read is on **A2** and the resolution of that pin is **8 bits**. An integer variable must be used from where the analogue value is printed from which must be a **10-bit** integer. After every serial print, a **delay** of **5 µS** must be implemented. The internal oscillator speed is **20 MHz**. Assume 1 clock cycle is equal to oscillation cycle. The serial print must happen on one single line only with text. Show all calculations. (9)

**[25]**

**QUESTION 2 VHDL QUESTIONS**

2.1 What does the following acronym stand for? (1)

FPGA

2.2 What three types of architectures can be used in VHDL programming? (3)

2.3 For the following identifiers (variables), decide which one is correct, and which one will produce a processor error. When there is an error, explain why it occurs. (3)

2.3.1 _step

2.3.2 sum20

2.4. There are three (3) non-decimal bit string numbers that can be used in VHDL.

For the decimal value of 246 predict will the three equivalent non-decimal bit string numbers be? (2 marks each) (6)

2.5 Design a NAND gate circuit diagram that uses MOSFETs. (4)

2.6 Differentiate between a signal and a variable with regards to *where it is declared* in a program and where it is visible in a process. (4)

| | **Variable** | **Signal** |
|---|---|---|
| **Place where it is declared** | | |
| **Visibility** | | |

2.7 Explain in your own words the advantages of using subprograms in VHDL? (5)

2.8 Compare two (2) of the four types of encoding that can be employed in finite state machines. (3 marks each) (6)

**[32]**

**QUESTION 3 VHDL QUESTIONS**

3.1 Compile the *truth table* and *implement the digital logic equation below in VHDL*. **ONE VHDL program** has to be compiled where dataflow and behavioural style have to be implemented on two different outputs. (No simplification of the equation may be performed) (20)

$$F_1 = AB + B\bar{C}D + \overline{A + \overline{B + D}}$$

| $A$ | $B$ | $C$ | $D$ | $AB$ | $\bar{C}$ | $B\bar{C}D$ | $B + D$ | $\overline{B + D}$ | $A+\overline{B + D}$ | $\overline{A + \overline{B + D}}$ | $F_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | | | | | | | |
| 0 | 0 | 0 | 1 | | | | | | | | |
| 0 | 0 | 1 | 0 | | | | | | | | |
| 0 | 0 | 1 | 1 | | | | | | | | |
| 0 | 1 | 0 | 0 | | | | | | | | |
| 0 | 1 | 0 | 1 | | | | | | | | |
| 0 | 1 | 1 | 0 | | | | | | | | |
| 0 | 1 | 1 | 1 | | | | | | | | |
| 1 | 0 | 0 | 0 | | | | | | | | |
| 1 | 0 | 0 | 1 | | | | | | | | |
| 1 | 0 | 1 | 0 | | | | | | | | |
| 1 | 0 | 1 | 1 | | | | | | | | |
| 1 | 1 | 0 | 0 | | | | | | | | |
| 1 | 1 | 0 | 1 | | | | | | | | |
| 1 | 1 | 1 | 0 | | | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | | | |

3.2 Compile a **VHDL program** to implement a timer in ***µs*** intervals. Start, stop and reset functionality must be implemented. Once 2 milliseconds have been reached, the timer must automatically reset. (23)

**[43]**

**TOTAL : 100**