UNIVERSITY OF JOHANNESBURG

PROGRAM	:	BACHELOR'S DEGREE B-ENG TECH *ENGINEERING: ELECTRICAL*
SUBJECT	:	**ELECTRONIC CIRCUITS A2**
CODE	:	**ELCELA2**
DATE	:	WINTER SSA EXAMINATION 2019 July 2019
DURATION	:	3 HOURS
WEIGHT	:	0.6
TOTAL MARKS	:	108

ASSESSOR	:	Mr. PJJ V ZYL
MODERATOR	:	Mr. J SEBASTIAN 2255
NUMBER OF PAGES	:	5 PAGES

INSTRUCTIONS	:	ANSWER ALL QUESTIONS IN THIS QUESTION PAPER. DO NOT USE ANY ADDITIONAL EXAM SCRIPT.
REQUIREMENTS	:	NONE

This Question paper must be handed in together with your script

SURNAME: _____ STUDENT NUMBER:_____

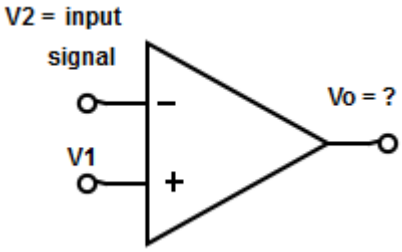
SIGNATURE: _____ this is to confirm that I am familiar with UJ's examination rules and procedures.

INSTRUCTIONS TO STUDENTS

1. ATTEMPT ALL QUESTIONS. 100 marks = 100%
2. THEORY TYPE QUESTIONS MUST BE ANSWERED IN POINT FORM BY CAREFULLY CONSIDERING THE MARK ALLOCATION.
3. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND IN PROPORTION.
4. ALL DIAGRAMS AND SKETCHES MUST BE LABELED CLEARLY.
5. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
6. NOTE: MARKS WILL BE DEDUCTED FOR WORK WHICH IS POORLY PRESENTED.
7. INSTRUCTIONS THAT ARE NOT ADHERED TO WILL BE SUBJECTED TO A PENALTY OF BETWEEN 50 AND 100 PERCENT OF THE MARKS ALLOCATED TO THE SPECIFIC QUESTION.

QUESTION 1

1.1 For an Op-Amp the following scenario exists.

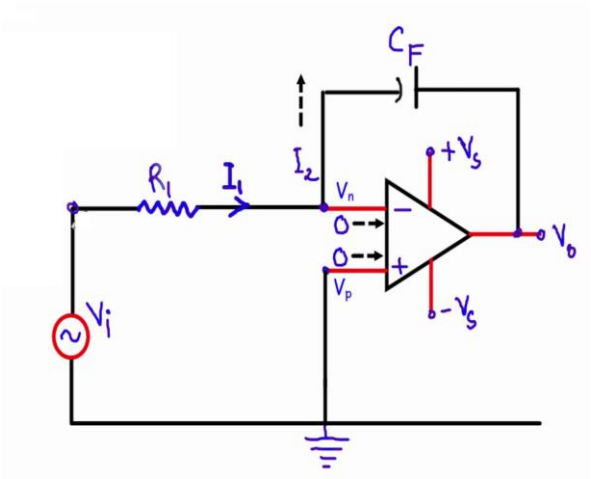


1.1.1 What is the output V_o if V1 is grounded? (2)

a) 180^0 in phase with input signal
b) 180^0 out of phase with input signal
c) Same as that of input signal
d) Output signal cannot be determined

1.1.2 Should gain be included for the above circuit, care must be taken because should the gain be too high it could cause the circuit to become _____ It is better to cascade two or more equal-gain stages than to attempt high gain in a single stage. In Instrumentation amplifiers non-loading of the circuit under test is required when low-level signals are measured. For this reason, these amplifiers use _____ amplifiers on the differential op-amp inputs. The quality of an amplifier can be defined by the ability to reject common input voltages. This is known as _____ (3)

1.2 Analyze the following figure to find the voltage at nodes V_n , V_p then formulate expressions for I_1 and I_2. (4)



1.3 Regarding a differential amplifier using an Op-Amp.
1.3.1 Sketch a neat drawing of a differential amplifier.
1.3.2 Formulate an equation for the output voltage showing the steps. [5]

1.4 For an Op-Amp integrator circuit.
1.4.1.1 Sketch an integrator, label it, and then derive an equation for Vout.
1.4.1.2 Should Vi = 10 x 10^{-3} sin 2000t, R = 1 M Ohm and C = 1 μF; find the output voltage at t1. Propose an application for this circuit. [7]

1.5 Make a sketch of an inverting amplifier with Rf = 1,2 MΩ, Ri = 50 kΩ, Vin = 0,1 Vrms volt and V^+ connected to ground. If the input signal's frequency is 100 kHz, determine if the amplifier can operate at this frequency if the maximum rated slew rate is 0,5 V/μS. (4)

1.6 Offset voltages and currents makes op-amps non-ideal.
1.6.1 What causes offset voltages?
1.6.2 How could one get rid of offset voltage? Explain using a practical sketch. (3)

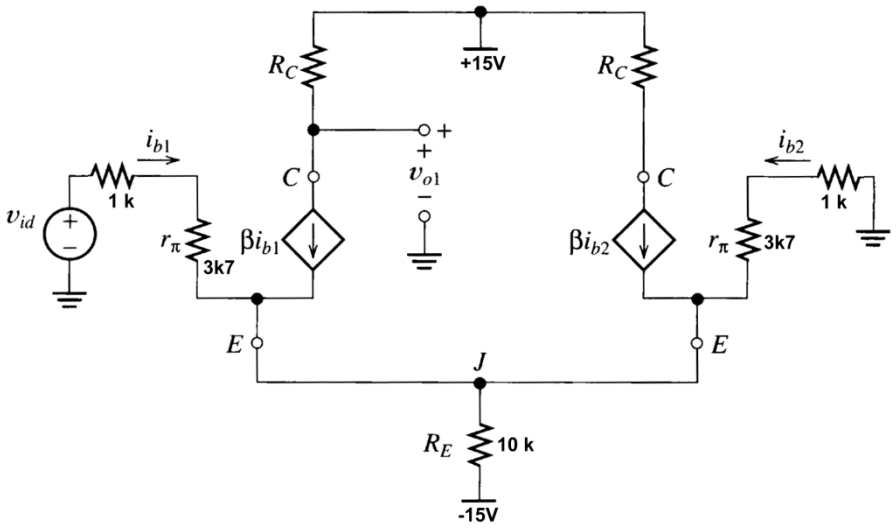
1.7 Positive Feedback. Identify 2 devices that utilizes positive feedback. (2)
[30]

QUESTION 2

2.1. Using a neatly drawn sketch derive an equation for the Common gain (A_c) of a discrete differential amplifier. (6)

2.2 A differential amplifier is shown on the next page. β 1 = β 2 = 100. Transistor admittance is 20 μS, R_C = 10 kΩ, R_B = 1 kΩ and Vid = 10 mV.

Replace RE with a transistor (β3 = 100; hoe = 20 μS) network to increase the CMRR of the amplifier. What is the CMRR now should Q3 be biased with 2 x 5 kΩ resistors? (10)



[16]

QUESTION 3

3.1 The Miller Theorem is a useful tool to convert series feedback impedances into parallel impedance. By formulations show how series feedback impedance can be replaced with a single impedance on the input side of the amplifier and a single impedance at the output side of the amplifier, labeled as Zm1 and Zm2. (6)

3.2 For a common emitter amplifier with Rb1, Rb2, Rc and Re. Sketch the high frequency small signal model and find the input and output miller capacitances (C_{mi} and C_{mo}). Take Cbe = 25 pF, Cbc = 2 pF, β = 100, Rc = 10 kΩ, gm = 33,3 mS and hie = 2.7 kΩ. (6)

3.3 A FET amplifier utilized in a high frequency environment has frequency poles at 900 kHz 1.5 MHz and 3 MHz. Estimate the approximate dominant -3dB high frequency cut off point for the amplifier. (5)

[17]

QUESTION 4

4.1 Design a BPF using Sallen-Key second-order active low and high-pass filters. If C = 0,01μF, calculate values for all the components used to give a total gain of 2.515. No DC balancing is required. Fc = 5 kHz and the bandwidth is 500 Hz. Sketch a detailed frequency/gain response curve. (12)

4.2 Illustrate how your design in Question 4.1 can be modified change the filter network into a notch filter (band-stop). (3)

4.3 Three most common filter characteristics are known as Butterworth, Chebyshev and Bessel, each giving a different response. Compile a table to compare the differences regarding to damping coefficient, shape of gain in the passband and stability. (9)

[24]

QUESTION 5

5.1 What is Voltage Series Feedback? (4)

5.2 With the aid of a block diagram formulate an equation for gain with feedback. (7)

5.3 Discuss the importance of negative feedback as applicable to amplifiers. (4)

[15]

QUESTION 6

6.1 According to transfer characteristics of a PLL, the phase error between VCO output & incoming signal must be maintained between _____ in order to maintain a lock.

a. 0 & π
b. 0 & π/2
c. 0 & 2π
d. π & 2π

6.2 Which characteristic of a PLL is defined as the range of frequencies over which the PLL can acquire lock with the input signal?

a. Free-running state
b. Pull-in time
c. Lock-in range
d. Capture range

6.3 In a PLL, the capture range is always _____the lock range.

a. Greater than
b. Equal to
c. Less than
d. None of the above

[6]

TOTAL = 108
