UNIVERSITY OF JOHANNESBURG

PROGRAM	:	NATIONAL DIPLOMA *ENGINEERING: ELECTRICAL*
SUBJECT	:	**ELECTRONICS 3**
CODE	:	**EEL341**
DATE	:	WINTER SSA EXAMINATION 2019 July 2019
DURATION	:	3 HOURS [08:00 to 11:00]
WEIGHT	:	0.6
TOTAL MARKS	:	100

ASSESSOR	:	Mr. HP VAN DER WALT
MODERATOR	:	Mr. J SEBASTIAN 2255
NUMBER OF PAGES	:	12 PAGES

INSTRUCTIONS	:	ANSWER ALL QUESTIONS IN THIS QUESTION PAPER. DO NOT USE ANY ADDITIONAL EXAM SCRIPT.
REQUIREMENTS	:	ONE EXAM SCRIPT FOR ROUGH WORK USE.

SURNAME:_____ STUDENT NUMBER:_____

SIGNATURE: _____ this is to confirm that I am familiar with UJ's examination rules and procedures.

INSTRUCTIONS TO STUDENTS

1. ATTEMPT ALL QUESTIONS. 100 marks = 100%
2. THEORY TYPE QUESTIONS MUST BE ANSWERED IN POINT FORM BY CAREFULLY CONSIDERING THE MARK ALLOCATION.
3. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND IN PROPORTION.
4. ALL DIAGRAMS AND SKETCHES MUST BE LABELED CLEARLY.
5. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
6. NOTE: MARKS WILL BE DEDUCTED FOR WORK WHICH IS POORLY PRESENTED.
7. INSTRUCTIONS THAT ARE NOT ADHERED TO WILL BE SUBJECTED TO A PENALTY OF BETWEEN 50 AND 100 PERCENT OF THE MARKS ALLOCATED TO THE SPECIFIC QUESTION.

QUESTION 1

1.1 Complete the missing words.

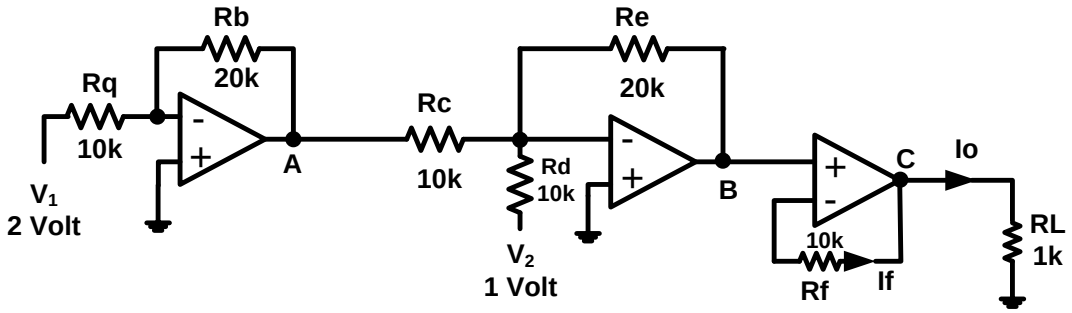
An ideal Operational Amplifier is basically a three-terminal device which consists of two _____ impedance inputs, one called the Inverting Input, marked with a negative or "minus" sign.

Should the gain be too high it could cause the circuit to _____ unless special care is taken during circuit design and PC board layout. It is better to cascade two or more equal-gain stages than to attempt high gain in a single stage.

Instrumentation amplifiers are used whenever DC gain is needed on a low-level signal that would be loaded by conventional differential-amplifier topologies. Instrumentation amplifiers take advantage of the _____ of non-inverting op-amp inputs.

Ideal Operational Amplifiers also have one output (although there are ones with an additional differential output) of _____ impedance that is referenced to a common ground terminal and it should ignore any common mode signals that is, if an identical signal is applied to both the inverting and non-inverting inputs there should be _____ change to the output. However, in real amplifiers there is always some variation and the ratio of the change to the output voltage with regards to the change in the common mode input voltage is called the _____ Rejection Ratio or CMRR. (3)

1.2 Analyze the following figure to find the voltage at nodes A, B and C. Determine the current Io and If. (6)



1.3 Regarding a discrete differential amplifier.
1.3.1 Sketch a neat drawing of such a differential amplifier using a LM741 OP-AMP.
1.3.2 Derive and formulate an equation for Vout should a 1 kΩ load resistor be connected to the output of the amplifier. [5]

1.4.1

1.4.1.1 Sketch an integrator, label it, and then derive an equation for Vout.

1.4.1.2 Should Vi = 10 x 10^{-3} sin 2000t, R = 1 M Ohm and C = 1 μF; find the output voltage at t1. Propose one application for this circuit. [7]

1.4.2 Regarding the construction of single and dual supplies for Op-Amps:

1.4.2.1 Sketch the circuit diagram of an inverting amplifier where a single battery is used to create a dual supply.

1.4.2.2 Repeat but illustrate how two batteries are used to create a dual supply voltage. [4]

1.5 Draw an inverting amplifier with Rf = 1,2 MΩ, Ri = 50 kΩ, Vin = 0,2 Vrms volt and v^+ connected to ground. If the input signal's frequency is 50 kHz, determine if the amplifier can operate at this frequency if the slew rate is 0,5 V/μS. (4)

1.6 Offset voltages and currents makes op-amps non ideal.

1. Define the offset voltage.

2. How could one reduce the effect of offset voltage? Illustrate using a sketch.

3. How could you reduce the effect offset currents? Illustrate using a sketch. (3)

1.7 Feedback.

1. Identify any op-amp application that utilizes positive feedback

2. Identify any op-amp application that utilizes negative feedback. (2)

[34]

QUESTION 2

Design a differential amplifier using 2 transistors VCC = -VEE = 15 V, Rc = 10k, $\beta = 100$, hoe = 20 μS, Rb1 = Rb2 = 1 kΩ. The common section only contains a single resistor (RE) = 10 kΩ. If IeQ = 715 μA find:

2.1.1 hie of Q1
2.1.2 The differential gain (Ad)
2.1.3 The common mode gain (Ac)
2.1.4 The CMRR of the amplifier
2.1.5 Output voltage if Vin = 10 mV rms (9)

2.2 Replace RE using a current source (providing the same bias current) implemented using a single BJT, and resistors only. (**Only illustrate this new section** and not the complete amplifier). (1)

2.3 Define and find the new CMRR of the improved circuit as in 2.2. (use the same parameters for Q3 as for Q1) (8)

[18]

QUESTION 3

3.1 An amplifier has feedback impedance Zf between input and output terminals. Derive equations to show how the feedback impedance can be replaced with a single impedance on the input side of the amplifier and a single impedance at the output side of the amplifier, labeled as Zm1 and Zm2. (6)

3.2 For a common emitter amplifier with Rb1, Rb2, Rc and Re. Sketch the high frequency small signal model and find the input and output miller capacitances (C_{mi} and C_{mo}). Take Cbe = 20 pF, Cbc = 2 pF, β = 100, Rc = 5k6, gm = 33,3 ms and βre (hie) = 3kΩ. (6)

3.3 A FET amplifier has R1 = R2 = 2 MΩ, RD = 10 kΩ, Rs = 1 kΩ, rds = 500 kΩ and a source (2 kΩ) connected to its input. Rs is bypassed with a 10 μF capacitor. If I_{DSS} = 10 mA, Vp = -4 V, V_{GSQ} = -1,5V, Cgd = 5 pF, and Cgs = 8 pF. Draw the small signal model and find:

3.3.1 Gm at the Q-point
3.3.2 The mid-band voltage gain
3.3.3 Values for the total in/output capacitances (11)

Question 3 (Continued)

3.3.4 The approximate dominant -3dB high frequency (5)

[28]

QUESTION 4

4.1 Create and design an active band-pass filter, making use of cascaded first order high and low-pass filters with a total gain of 12. The centre frequency must be 1100 Hz and the bandwidth equal to 1800 Hz. Sketch a neat graph (freehand) to show the response of the filter. Use C = 0,01 μF. Indicate the dB levels as well as all frequencies. No DC balancing is required. (6)

4.2 Design a second order active HPF where R1 = R2 = R = 10 kΩ, C1 = C2 = C = 0,1 μF, Rf = 5k8 and Ri = 10 kΩ.

4.2.1 What is the 3dB frequency below the pass-band value?
4.2.2 What is the gain in the pass-band?
4.2.3 What is the response of this filter (type)? (5)

4.3 Show how your design in question 4.1 can be modified change the filter network into a notch filter (band-stop). (3)

4.4 Compare the advantages of active filters to passive filters. (4)

[18]

QUESTION 5

5.1 Discuss the importance of negative feedback as applicable to amplifiers. (5)

5.2 Sketch the block diagram of a typical PLL system. Indicate the phase relationships that exist between the different blocks (2)

[7]

TOTAL = 105