UNIVERSITY OF JOHANNESBURG

PROGRAM	:	NATIONAL DIPLOMA *ENGINEERING: ELECTRICAL*
SUBJECT	:	**DIGITAL SYSTEMS 2**
CODE	:	**EDS 231**
DATE	:	SUMMER EXAMINATION 2017 16 NOVEMBER 2017
DURATION	:	(SESSION 2) 12:30 - 15:30
WEIGHT	:	40:60

ASSESSOR	:	Mr. V Rameshar
MODERATOR	:	Mr. D.R. Van Niekerk
NUMBER OF PAGES	:	PAGES 4
FULL MARKS	:	100

INSTRUCTIONS TO STUDENTS

1. ATTEMPT ALL QUESTIONS. 100 marks = 100%
2. THEORY TYPE QUESTIONS MUST BE ANSWERED IN POINT FORM BY CAREFULLY CONSIDERING THE MARK ALLOCATION.
3. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND IN PROPORTION.
4. ALL DIAGRAMS AND SKETCHES MUST BE LABELED CLEARLY.
5. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
6. NOTE: MARKS WILL BE DEDUCTED FOR WORK, WHICH IS POORLY PRESENTED.

QUESTION 1

1.1 Provide the full names of the following:-

1.1.1 DTL
1.1.2 CMOS
1.1.3 RTL
1.1.4 DL (4)

1.2 With the use of TTL diagrams, explain current source and current sink. Label the sink/source current values and Fan-out capabilities for TTL (7400). (8)

1.3 Show with the aid of a sketch how you would interface a 7-segment display. Provide all labels. (4)

[16]

QUESTION 2

2.1 Sketch an asynchronous 2 bit up counter using positive edge triggered J-K flip/flop IC's. Provide a suitable truth table. (8)

2.2 Design a synchronous 3-bit down counter from 1st principles using J-K flip flops and K-Maps. Please utilise transition table below. All steps must be shown. (14)

$Q \rightarrow Q_{n+1}$	J	K
$Q \rightarrow Q$	0	d
$Q \rightarrow 1$	1	d
$1 \rightarrow Q$	d	1
$1 \rightarrow 1$	d	0

2.3 Sketch the timing diagram for a twisted ring counter and indicate on it how you get to a MOD-10. (6)

2.4 Data is loaded into a shift register in two main forms, either parallel or series. With the aid of a sketch, show how a parallel in series out shift register would move 4 bits of data in and out. How many clock pulses would make this possible? (6)

[34]

QUESTION 3

3.1 If a 555 timer is configured to run in the a-stable mode (oscillator) when

$V_{CC} = 6.5$ V; C = 0,133 μf; R1 = 3,7 kΩ and $R_2 = 4,7$ kΩ.

Calculate the following:

3.1.1 T_H
3.1.2 T_L
3.1.3 Frequency
3.1.4 Duty cycle. (8)

3.2 Make a neat-labeled sketch of the internal parts of a 555 timer IC. (5)

3.3 Pulsed circuits may be triggered manually or automatically. By the use of timing, diagrams explain the difference between triggerable and non-retriggerable mono-stables by referring to 74121 and 74122 IC's. (8)

[21]

QUESTION 4

4.1 Describe a RAM and ROM (4)
4.2 Explain the meaning of Dynamic and Static memory. (4)
4.3 How would you describe noise and noise immunity? (4)
4.4 How would a unused TTL input act if it is open? (2)
4.5 How can a TTL circuit be interfaced with a CMOS circuit? (2)

[16]

QUESTION 5

5.1 Sketch a 4-bit R/2R DAC (digital-to-analog converter). Show all resistor ratio values. (5)

5.2 Sketch a successive approximation (analog-to-digital convertor). (8)

[13]

TOTAL = 100