UNIVERSITY OF JOHANNESBURG

PROGRAM	:	NATIONAL DIPLOMA *ENGINEERING: ELECTRICAL*
SUBJECT	:	**DIGITAL SYSTEMS 2**
CODE	:	**EDS 231**
DATE	:	SUMMER EXAMINATION 2016 24 NOVEMBER 2016
DURATION	:	(SESSION 2) 12:30 - 15:30
WEIGHT	:	40:60

ASSESSOR	:	Mr. V Rameshar
MODERATOR	:	Mr. D.R. Van Niekerk
NUMBER OF PAGES	:	PAGES 4
FULL MARKS	:	100

INSTRUCTIONS TO STUDENTS

1. ATTEMPT ALL QUESTIONS. 100 marks = 100%
2. THEORY TYPE QUESTIONS MUST BE ANSWERED IN POINT FORM BY CAREFULLY CONSIDERING THE MARK ALLOCATION.
3. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND IN PROPORTION.
4. ALL DIAGRAMS AND SKETCHES MUST BE LABELED CLEARLY.
5. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
6. NOTE: MARKS WILL BE DEDUCTED FOR WORK WHICH IS POORLY PRESENTED.

QUESTION 1

1.1 If a 555 timer is configured to run in the a-stable mode (oscillator) when

V_{CC} = 5 V; C1 = 0,021 µf; R1 = 3,3 kΩ and R_2 = 3,9 kΩ.

Calculate the following values:

1.1.1 t_H
1.1.2 t_L
1.1.3 frequency
1.1.4 duty cycle. (8)

1.2 Calculate the 555 Monostable multivibrator time period for the circuit with R_A = 7.5 kΩ and C = 0.02 µF. (4)

1.3 A certain application requires a one-shot with a pulse width of approximately 100 ms. Using a 74121, calculate the component values. Select R_{EXT} = 39 kΩ and calculate the necessary capacitance. (6)

1.4 Use timing diagrams to explain the difference between triggerable and non-retriggerable mono-stables by referring to 74121 and 74122 IC's. (8)

[26]

QUESTION 2

2.1 Sketch an asynchronous MOD-10 up counter using negative edge triggered J-K flip/flop IC's. Give the truth table and show which code is detected. (8)

2.2 Design a synchronous Mod-10 up counter from 1st principles using K-MAPS.
Use Diagram 1 (*insert in answer book*) (14)

2.3 Sketch a MOD-10(5-bit) Johnson counter using D-bistables. Sketch the timing diagram for the counter and indicate on it how you get to a MOD-10. (6)

2.4 Sketch a 4-bit *parallel in-serial out* shift register using D-bistables. The shift register make use of a *SHIFT / $\overline{LOAD}$* input (using NAND gates) to put data parallel in and to move data serial out. Sketch the logic symbol for the shift register. (6)

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QUESTION 3

3.1 A certain gate draws a DC supply current from a +5 V source of 2 mA in the low state and 3,4 mA in the high state. What is the average power dissipation? We have a duty cycle of 50%. (4)

3.2 Use logic gate diagrams to explain current sinking and current sourcing. Give the sink/source current values and Fan-out capabilities for TTL (7400). (6)

[10]

QUESTION 4

4.1 List two types of RAM memory. (2)
4.2 What is a *cache* memory? (1)
4.3 Describe the refresh operation in a DRAM memory. (3)
4.4 List the types of read-only memories (ROMs). (4)
4.5 Describe the loading and erasing of data of the memories in Q 4.4. (4)

[14]

QUESTION 5

5.1 Sketch a 4-bit (A) Binary Weighted and (B) R/2R DAC (digital-to-analog converter). Show all resistor ratio values. (8)

5.2 Sketch and explain how a FLASH *ADC* (analog-to-digital convertor) works. (8)

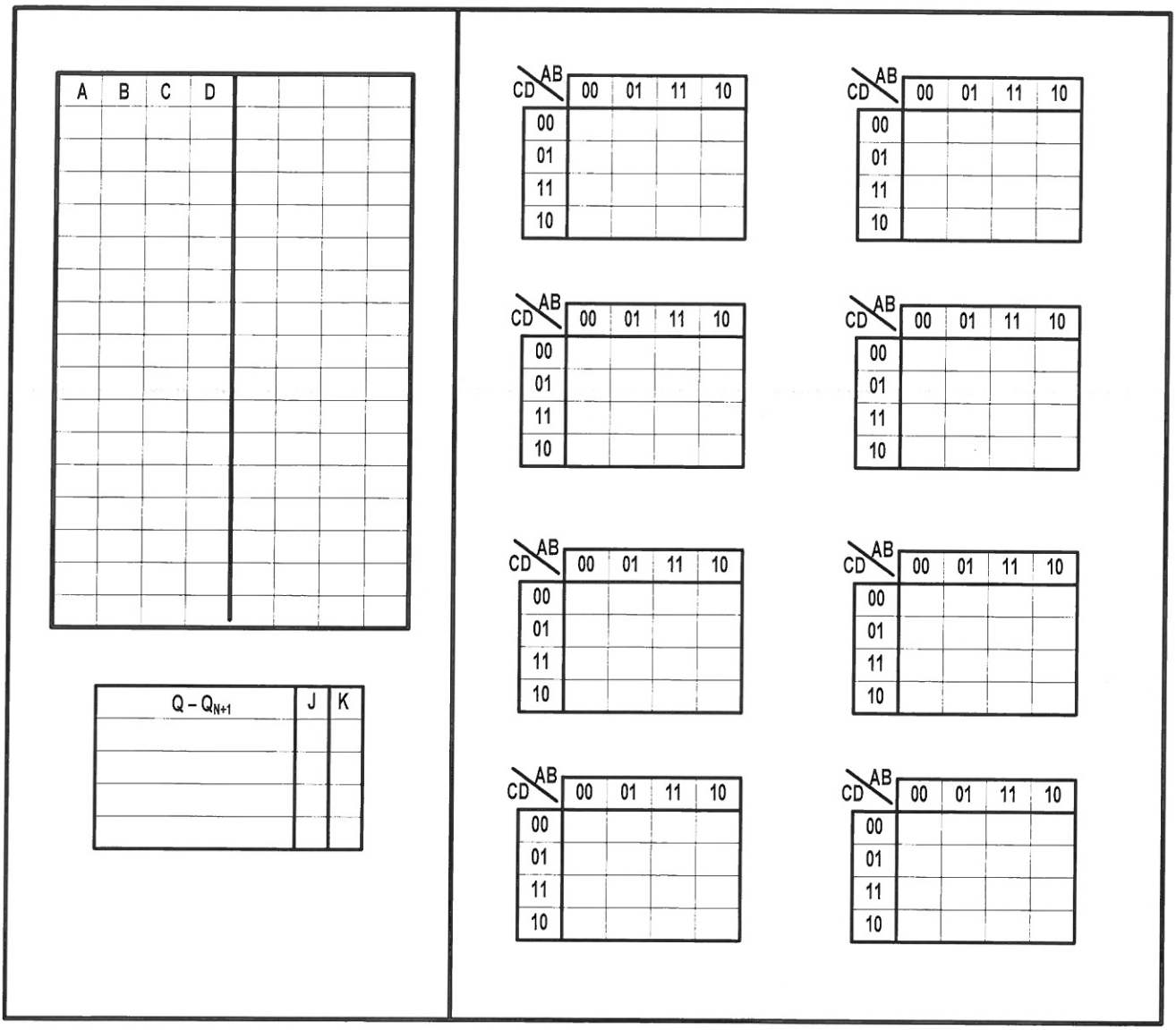
[16]

TOTAL = 100

STUDENT SURNAME: _____

STUDENT NUMBER: _____

DIAGRAM 1



SKETCH A SYNCHRONOUS COUNTER BELOW: