

PROGRAM : NATIONAL DIPLOMA

ENGINEERING: COMPUTER SYSTEMS

ENGINEERING: ELECTRICAL

SUBJECT : DIGITAL SYSTEMS 1

<u>CODE</u> : **EDS121**

DATE : 29 July 2016

WINTER SSA Examination

<u>DURATION</u> : 08:00 - 11:00

<u>WEIGHT</u> : 40 : 60

TOTAL MARKS : 100

ASSESSOR : MR V Rameshar

MODERATOR : MR D.R. Van Niekerk

NUMBER OF PAGES : 3 PAGES

INSTRUCTIONS

1. NO CALCULATORS ALLOWED

2. ALL SKETCHES MUST BE NEAT AND FULLY LABELLED.

QUESTION 1

Calculate in binary and then follow the instructions for each question:

- 1.1 $23_8 + 6E_{16}$ (Convert your answer to Decimal) (6)
- 1.2 $225_8 13_{10}$ (Convert your answer to Hexadecimal) (6)
- 1.3 10101×1001 (Convert your answer to Octal) (6)
- 1.4 $1100010 \div 1101$ (6)

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QUESTION 2

- 2.1 Sketch the symbol and provide a truth table for each of the following logic gates below: -
 - 2.1.1 Half Subtractor
 - 2.1.2 NOR
 - 2.1.3 NAND

(9)

2.2 Sketch the circuit equivalent of the following equations below and provide the equivalent Boolean expressions output: -

$$2.2.1 \quad AB + \overline{AB} \tag{6}$$

$$2.2.2 \quad \overline{\overline{CD}}$$
 (6)

2.3 By using NOR gates only simplify sketch the logic gate circuit diagram. (Use de Morgans theorem)

$$F = A\overline{B}C + A\overline{B}D + (\overline{A}C + \overline{D})$$
(10)

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QUESTION 3

3.1	By the use of parity bits and the given data 101101, prepare the transmission using hamming code. ODD parity should be used. Show	
	all steps.	(10)
3.2	Why are parity checks performed in data transmission?	(3)
3.3	How many bits are there in a kilobyte of data	(2)
		[14]
QUESTION 4		
4.1	Give the binary equivalent of 11101 Gray code.	(3)
4.2	Expand the acronym ASCII and provide one use the code?	(3)
4.3	What is the excess-3 equivalent of 543?	(2)
4.4	Explain weighted and unweighted codes.	(4)
4.5	Sketch two forms of digital signals and provide detailed labels.	(4)
4.6	Indicate how sign bits are used in the binary number system.	(2)
4.7	Explain with aid of sketches debounced and not debounced digital signals	(4)
		[<u>22</u>]

QUESTION 5

Sketch a 1 to 4 demultiplexer circuit showing its input and output on a truth table. The circuit must be clearly labeled and neat.

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