UNIVERSITY OF JOHANNESBURG

PROGRAM	:	NATIONAL DIPLOMA *ENGINEERING: ELECTRICAL*
SUBJECT	:	**DIGITAL SYSTEMS 2**
CODE	:	**EDS 231**
DATE	:	SUMMER SSA EXAMINATION 2017 13 JANUARY 2017
DURATION	:	(SESSION 1) 08:00 - 11:00
WEIGHT	:	40:60

ASSESSOR	:	Mr. V Rameshar
MODERATOR	:	Mr. D.R. Van Niekerk
NUMBER OF PAGES	:	PAGES 6
FULL MARKS	:	100

INSTRUCTIONS TO STUDENTS

1. ATTEMPT ALL QUESTIONS. 100 marks = 100%
2. THEORY TYPE QUESTIONS MUST BE ANSWERED IN POINT FORM BY CAREFULLY CONSIDERING THE MARK ALLOCATION.
3. ALL DIAGRAMS AND SKETCHES MUST BE DRAWN NEATLY AND IN PROPORTION.
4. ALL DIAGRAMS AND SKETCHES MUST BE LABELED CLEARLY.
5. ALL WORK DONE IN PENCIL EXCEPT DIAGRAMS AND SKETCHES WILL BE CONSIDERED AS ROUGH WORK.
6. NOTE: MARKS WILL BE DEDUCTED FOR WORK WHICH IS POORLY PRESENTED.

QUESTION 1

1.1 Define the following terms with reference to TTL:
1.1.1 Noise margin
1.1.2 Speed/power relation
1.1.3 Fan-out
1.1.4 Sink current
1.1.5 Propagation delay time. (5)

1.2 A certain gate draws 2 mA when its output is HIGH and 3.6 mA when its output is LOW. What is its average power dissipation if V_{CC} is 5 V and the gate is operated on a 50% duty cycle? (5)

1.3 Determine the value for the pull-up resister for an open-collector gate if $I_{OL(max)}$=40 mA and $V_{OL(max)}$=0.25 V for each gate. Assume that 10 standard TTL unit loads are being driven from output X and the supply voltage is 5 V. (6)

[16]

QUESTION 2

2.1 Explain the term 'retriggerable one-shot' and also show the result on a timing diagram. (3)

2.2 An output pulse of 1000 ns duration is to be generated by a 74122 one-shot. Using a capacitor of 560 pF, determine the value of external resistance required. (5)

2.3 Design and Sketch a one-shot, using a 555 timer that will produce a 0.25 s output pulse. (C_1 = 1 μF) (3)

[11]

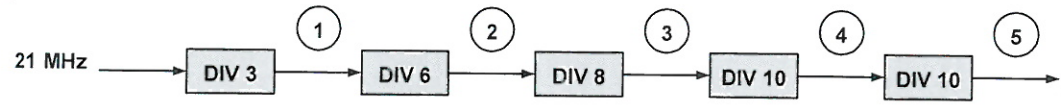
QUESTION 3

3.1 How does a synchronous counter differ from an asynchronous counter? (1)

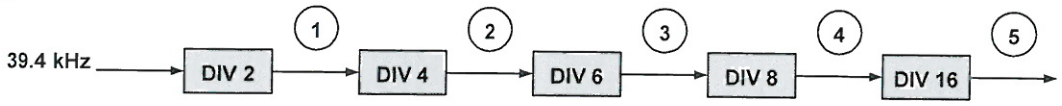
3.2 Design a synchronous counter to produce the following binary sequence. Use J – K flip-flops. Answer on the annexure sheet provided.
1, 4, 3, 5, 7, 6, 2, … (18)

3.3 For each of the cascaded counter configurations, determine the frequency of the waveform at each point indicate by a circled number, and determine the overall modulus.

a) (5)



b) (5)



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QUESTION 4

4.1 Why are shift registers considered as basic memory devices? (2)

4.2 What is the storage capacity of a register that can retain two bytes of data? (2)

4.3 A divide-by-10 ring counter requires a minimum of:

a) ten flip-flops
b) five flip-flops
c) four flip-flops
d) twelve flip-flops (2)

4.4 Sketch the logic diagram for a four-bit Johnson counter and also Sketch the timing sequence for the counter. (Twisted ring). (10)

[16]

QUESTION 5

5.1 The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is

a) 1024
b) 8192
c) 8
d) 4096 (1)

5.2 A 32-bit data word consist of
a) 2 bytes
b) 4 nibbles
c) 4 bytes
d) 8 bytes (1)

5.3 Data is stored in RAM during the
a) read
b) enable
c) write
d) addressing operation (1)

5.4 Data that is stored at a given address in RAM is lost when
a) power goes off
b) data is read from the address
c) new data are written at the address
d) both (a) and (c) (1)

5.5 A ROM is a
a) non-volatile
b) volatile
c) read/write
d) byte-organized memory. (1)

5.6 The storage cell in a SRAM is
a) a flip-flop
b) a capacitor
c) a fuse
d) a magnetic domain. (1)

5.7 A DRAM must be
a) replaced periodically
b) refreshed periodically
c) always enabled
d) programmed before each use. (1)

5.8 What is the *smallest unit* of information that can be stored in a memory? (1)

5.9 What is a *write* operation? (1)

5.10 What is a *read* operation? (1)

5.11 Describe the difference between a RAM and a ROM. (2)

5.12 Describe the refresh operation in a DRAM. (2)

[14]

QUESTION 6

6.1 Sketch the R/2R D-A convertor *and* show its resistor ratios values. (6)

6.2 Explain with the aid of sketches how the Successive-Approximation conversion process takes place when receiving an analog voltage of 5V on the input. (Use the Keep/Reset method). (8)

[14]

TOTAL MARKS = 100

ANNEXURE

STUDENT NUMBER _____ **SURNAME**_____

STUDENT_SURNAME_____

NEXT STATE TABLE

Present State Q_2 Q_1 Q_0	Next State Q_2 Q_1 Q_0

TRANSMISSION TABLE

Output State Transitions (Present state to next state) Q_2 Q_1 Q_0	Flip-flop inputs J_2 K_2 J_1 K_1 J_0 K_0