UNIVERSITY OF JOHANNESBURG

PROGRAM	:	NATIONAL DIPLOMA *ENGINEERING: COMPUTER SYSTEMS* *ENGINEERING: ELECTRICAL*
SUBJECT	:	**DIGITAL SYSTEMS II**
CODE	:	**EDS231**
DATE	:	SUMMER EXAMINATION 2015 19 NOVEMBER 2015
DURATION	:	(SESSION 2) 12:30 - 15:30
WEIGHT	:	40: 60
TOTAL MARKS	:	100
ASSESSOR	:	MR J A NIEUWOUDT
MODERATOR	:	MR V RAMESHAR
NUMBER OF PAGES	:	3 PAGES AND 1 ANNEXURE

2247

INSTRUCTIONS :

1. ONE CALCULATOR MAY BE USED.
2. ATTEMP ALL QUESTIONS
3. ALL STEPS MUST BE SHOWN
4. UNTIDY WORK WILL BE PENALISED
5. WITH THE EXCEPTION OF SKETCHES ALL WORK MUST BE DONE IN PEN.
6. **NB**: HAND IN DIAGRAM 1 WITH ANSWER SHEET

REQUIREMENTS : NONE

QUESTION 1

1.1 When is a pull-up resistor required when interfacing TTL and CMOS? (1)

1.2 Explain with *drawings* how you will be handling unused TTL inputs. (4)

1.3 In what output state does a TTL circuit sink current from the load? (1)

1.4 An unconnected TTL input acts as a LOW. (T or F) (1)

[7]

QUESTION 2

2.1 Explain the term 'non-retriggerable one-shot' and also clearly show the result on a timing diagram. (4)

2.2 A certain application requires a one-shot with a pulse width of approximately 100 ms. Using a 74121 mono-stable, **show** the connections **and** calculate the component values. Select R_{EXT} = 39 kΩ and calculate the necessary capacitance. (6)

2.3 Design a *one-shot*, using a 555 timer that will produce a 0.25 sec output pulse. (Use C_1 = 1 µF). Draw the block *diagram* to show how the external components are connected. (6)

[16]

QUESTION 3

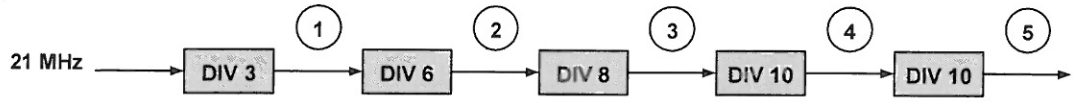
3.1 How do synchronous and asynchronous counters differ? (1)

3.2 Show how the 74LS93A counter IC can be used as a (1) MOD 13 and (2) MOD 15 counters. (Show only external connection layout). (6)

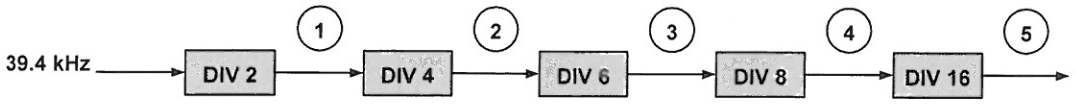
3.3 *Design* and *Draw* a *synchronous* counter to produce the following binary sequence. Use J – K flip-flops. Answer on the annexure sheet (Diagram1) provided. 1, 4, 3, 5, 7, 6, 2, 0, … (14)

3.4 For each of the cascaded counter configurations, determine the frequency of the waveform at each point indicate by a circled number, and determine the overall modulus. (10)

a)



b)



[31]

QUESTION 4

4.1 Why are shift registers considered as basic memory devices? (2)

4.2 What is the storage capacity of a register that can retain two bytes of data? (2)

4.3 A MOD 10 *Ring* counter requires a minimum of:
a) ten flip-flops
b) five flip-flops
c) four flip-flops
d) twelve flip-flops (1)

4.4 Draw the *logic* diagram for a four-bit *Johnson* counter and also draw the *timing* diagram for the counter. (6)

4.5 Draw a single 4-bit shift register that have a *Parallel* data in loaded and *serial* data out, but also have the facility to load data out *parallel* with an enable /shift pulse through AND /OR gates. (6)

[17]

QUESTION 5

5.1 Draw the 2^s **complemen*ting*** circuit. (4)

5.2 Draw and explain how a Successive-Approximation analog-to-digital convertor works. (Give drawings to show how the end result is achieved). (8)

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QUESTION 6

6.1 What is the smallest unit of data that can be stored in a memory? (1)

6.2 What is the bit capacity of a memory that can store 256 bytes of data? (1)

6.3 What is a write operation? (1)

6.4 What is a read operation? (1)

6.5 How is a given unit of data located in a memory? (1)

6.6 Describe the difference between a RAM and a ROM. (2)

6.7 Explain how SRAMs and DRAMs differ. (2)

6.8 Draw and explain how a FLASH MEMORY when programed is storing (i) a logic 1 and (ii) a logic 0. (8)

[17]

TOTAL MARKS = 100

DIAGRAM 1

DIGITAL SYSTEMS 2

STUDENT SURNAME: ____________________ STUDENT NUMBER: ________

CURRENT			NEXT		
A	B	C	W	X	Y

OUTPUT	TRANSITION	FLIP-FLOP	INPUTS
Qn	Qn + 1	J	K

	0	1
00		
01		
10		
11		

	0	1
00		
01		
10		
11		

	0	1
00		
01		
10		
11		

	0	1
00		
01		
10		
11		

	0	1
00		
01		
10		
11		

	0	1
00		
01		
10		
11		

DRAW THE SYNCHRONOUS COUNTER HERE